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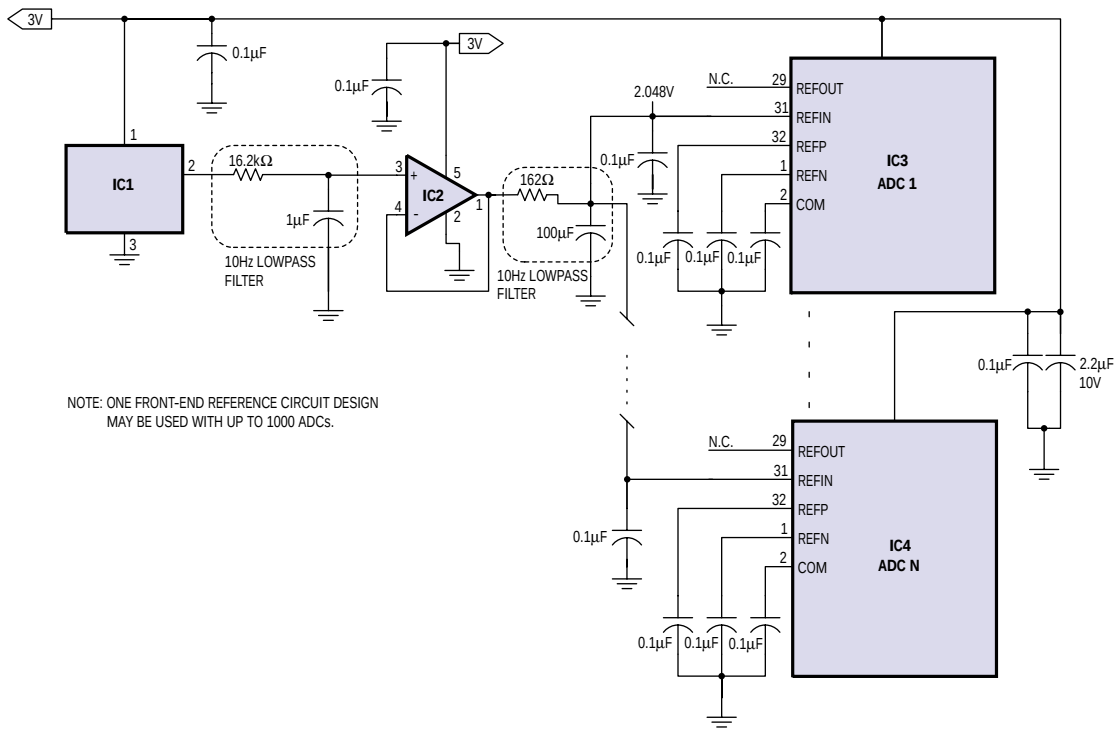
LOW-NOISE REFERENCE CIRCUIT



For ultrasound applications, a single, low-noise reference circuit drives up to 1000 ADCs. (See article inside, page 3.)

News Briefs

MAXIM REPORTS REVENUES AND EARNINGS FOR THE SECOND QUARTER OF FISCAL 2002

Maxim Integrated Products, Inc., (Nasdaq: MXIM) reported net revenues of $247.1 million for its fiscal second quarter ending December 29, 2001, down from the $438.3 million reported for the second quarter of fiscal 2001 and up from the $239.4 million reported for the first quarter of fiscal 2002. Net income for the quarter was $62.6 million, a decrease from the $122.2 million reported last year and an increase over the $61.3 million reported for the previous quarter. Diluted earnings per share were $0.18 for the second quarter, down from the $0.34 reported for the same period a year ago and up from the $0.17 reported for the first quarter of fiscal 2002.

During the quarter, cash and short-term investments increased $22.1 million after the Company repurchased 2.0 million shares of its common stock for $67.8 million and acquired a total of $18.7 million of capital equipment. The stock repurchase was enabled by temporary suspension by the SEC of regulations relating to stock repurchases after pooling-of-interests transactions. Accounts receivable decreased by $4.7 million in the second quarter to $94.8 million, and inventories decreased $4.9 million to $154.4 million.

Gross margin for the second quarter increased slightly to 70.1%, after increasing inventory reserves $3.0 million, compared to 70.0% reported for the first quarter. Research and development expense increased from the $66.0 million reported in the first quarter or 27.6% of net revenues to $68.6 million or 27.7% of net revenues, primarily the result of hiring additional engineers and investing in new product development. Selling, general and administrative expenses decreased from $25.1 million in the first quarter to $22.9 million in the second quarter, primarily due to control of discretionary spending.

Second quarter bookings were approximately $230 million, a 9% increase over the first quarter's level of $211 million. Turns orders received during the quarter were $125 million, a 23% increase over the $102 million received in the prior quarter (turns orders are customer orders that are for delivery within the same quarter and may result in revenue within the same quarter if the Company has available inventory that matches those orders). Order cancellations were down 39% from the first quarter and down 81% from the year ago level. Bookings increased in all geographic regions except the U.S., where bookings decreased slightly compared to the prior quarter. Bookings increased in most of the Company's 14 business units, with particular strength in those business units with products for portable equipment. Bookings were down from the first quarter for those business units with products for the test equipment, fiber, and telecommunication equipment markets.

Second quarter ending backlog shippable within the next 12 months was approximately $187 million, including $170 million requested for shipment in the third quarter of fiscal 2002.

Jack Gifford, Chairman, President, and Chief Executive Officer, commented on the quarter: "We are encouraged by the continued increase in bookings during our second quarter. Although visibility remains limited, we currently expect bookings to increase again in our third quarter."

Mr. Gifford continued: "We are confident that inventory levels for much of the end equipment that our products address are either significantly reduced or have moderated. We remain cautious about the short-term outlook for the telecom and ATE markets, where our customers are still working through inventories. Although we believe that our customers' visibility is better now than it has been in the past several quarters, turns orders remain high because of our short lead times. As lead times increase, we expect customers to place orders beyond their immediate needs."

Mr. Gifford concluded: "Unlike some companies in our industry, Maxim has continued to increase its engineering headcount and its investment in research and development activities. In our second quarter, R&D expenses were nearly 28% of net revenues, a historically high level for the Company and a remarkably high level for any mature company in our industry."

Certain statements in this press release are forward-looking statements within the meaning of the Private Securities Litigation Reform Act of 1995. These statements involve risk and uncertainty. All forward-looking statements included in this news release are made as of the date hereof, based on the information available to the Company as of the date hereof, and the Company assumes no obligation to update any forward-looking statement.

Maxim Integrated Products is a leading international supplier of quality analog and mixed-signal products for applications that require real world signal processing.

Reference voltage for multiple ADCs

Ultrasound-imaging systems usually host a large array of analog-to-digital converters (ADCs). Not only do these systems require precise channel-to-channel matching, but also a careful design of the voltage reference system in order to maintain sufficient dynamic performance.

These reference systems typically provide a precise, low-noise reference to a large bank of converters. To further ensure accuracy and stability, the ADCs' reference inputs should be buffered to minimize the loading effects on the reference system. In response to these requirements, high-speed ADC manufacturers have begun supplying converters with reference inputs that can support the use of both the internal precision reference and an external, precision, reference-voltage source.

Medical ultrasound-imaging systems, for example, commonly use a large number of ADCs in the receiver's beamforming electronics, usually organized in groups of 16, 24, 32, etc. Maximum beam accuracy requires the absolute minimum beamforming path errors. A major source of these errors can be traced to poor accuracy in terms of noise and the actual reference voltage present at each of the individual ADCs. Other error sources include variances in the distributed load seen by the reference's source. In any particular system architecture, this load can consist of the many individual resistive and capacitive loads seen by the reference. Several approaches can provide the reference voltage for such ADC arrays:

- **Individual on-chip references.** Though it offers a convenient connection locally to each ADC, this option features relatively poor matching between the converters.
- **A single, external reference voltage applied to all reference inputs of the ADC array.** Such a configuration allows the user to engineer an external reference voltage of arbitrary accuracy, but incurs error due to small variations among the resistor ladders (one ladder internal to each ADC).
- **An external reference driving the ADCs' reference-ladder taps directly.** This option delivers maximum gain accuracy by directly controlling the reference voltage applied to each ADC ladder. However, it requires driving the (relatively) low resistance of the ladders, and some ADCs do not allow access to that internal bias point.

ADC accuracy

For many applications, gain and noise level have a major effect on ADC accuracy. The gain of an ADC is represented by the slope of its transfer function, which relates analog inputs to the allowable range of digital output codes. One way to quantify gain is to measure the full-scale (FS) input range, which is directly controlled by the reference-voltage level. For medical ultrasound imaging systems, variation in the full-scale range of the ADCs can cause errors in beam formation. It also varies the ADCs' clipping point—an effect that may be important in certain signal-demodulation schemes.

An ADC's noise level determines its useable dynamic range; this dynamic range should generally be as large as possible. The reference-noise component of ADC noise can be additive or multiplicative. Additive noise is easily filtered by local bypass capacitors on the individual ADCs, which in most designs are already present to optimize the ADC's dynamic performance.

Multiplicative noise, on the other hand, is more insidious. For ultrasound applications, reference noise in the audio frequency spectrum can modulate large "stationary" signals in the RF spectrum. Such signals are produced by stationary tissue in the ultrasound target. Audio modulation produces sidebands on the RF signal that can be demodulated by a Doppler detector, producing audio tones in the detected Doppler output signal.

To estimate the amount of audio noise tolerable in an ultrasound application, assume a nearly full-scale RF signal applied to a 10-bit ADC like the MAX1448. The dynamic range of that device (almost 60dB) implies a noise floor of -60dBFS. That noise level can be normalized to a 1Hz bandwidth. The Nyquist bandwidth for an 80MHz sampling rate is 40MHz. The correction factor is $\sqrt{40MHz}$ = 76dB, which places the ADC's noise floor at -60dBFS - 76dBFS = -136dBFS. Because a conservative design requires the reference-voltage noise to be at least 20dB lower (-156dBFS), a 2.0V reference requires an extremely low noise level of $33nV_{P-P}$ (approximately $8nV_{RMS}/\sqrt{Hz}$).

A multi-ADC array may require a reference voltage more accurate than the one internal to each converter (the reference internal to MAX144x converters, for example, is ±1% accurate). The following two circuits are submitted as reference designs for such arrays. They feature a single, common low-frequency noise filter, and they achieve high-frequency noise suppression with local decoupling capacitors on individual ADCs.

Single external reference

Multiple-converter systems based on the MAX144x (IC3, IC4) family are well-suited for use with a common reference voltage. The REFIN pin of those converters can be connected directly to an external reference source, eliminating the need for any circuit modification. Moreover, the high input impedance of REFIN (even of multiple REFIN terminals connected in parallel) draws only a small load current.

A precision source like the MAX6062 (IC1) generates an external DC level of 2.048V **(Figure 1)**, and exhibits a noise-voltage density of 150nV/√Hz. Its output passes through a 1-pole lowpass filter (with 10Hz cutoff frequency) to an op amp (IC2) like the MAX4250, which buffers the reference before its output is applied to a second 10Hz lowpass filter. IC2 provides a low offset voltage (for high-gain accuracy) and a low noise level. The passive 10Hz filter following the buffer attenuates noise produced in the voltage-reference and buffer stages. This filtered-noise density, which decreases for higher frequencies, meets the noise levels specified for precision ADC operation.

Converters of the MAX144x family are specified for a typical gain error of ±4.4% (better than ±0.5dB). This performance is better than the gain tolerance of all other building blocks in the signal path of an ultrasound receiver. Note that proper power-up/down sequencing is ensured because all active parts are driven from the same supply voltage. That approach yields excellent gain matching and a very low noise level with minimal circuitry and should suffice in many applications that require multiple gain-matched ADCs.

Generating a precision external reference

For applications requiring more stringent gain matching **(Figure 2)**, the MAX144x family again is well suited. Connecting each REFIN to analog ground disables the internal reference of each device, allowing the internal reference ladders to be driven directly by a set of external reference sources. These voltages can have an arbitrarily tight tolerance, and the ADCs track them within 0.1% (typ). ADCs of this family also feature a 4kΩ resistance across the ladder reference connection, which allows the load to be easily driven even with many ADCs in parallel.

A DC level of 2.500V can be generated by a precision source (IC1) such as the MAX6066, followed by a 10Hz lowpass filter and precision voltage divider. The buffered outputs of this divider are set to 2.0V, 1.5V, and 1.0V, with an accuracy that depends on the tolerance of the divider resistors.

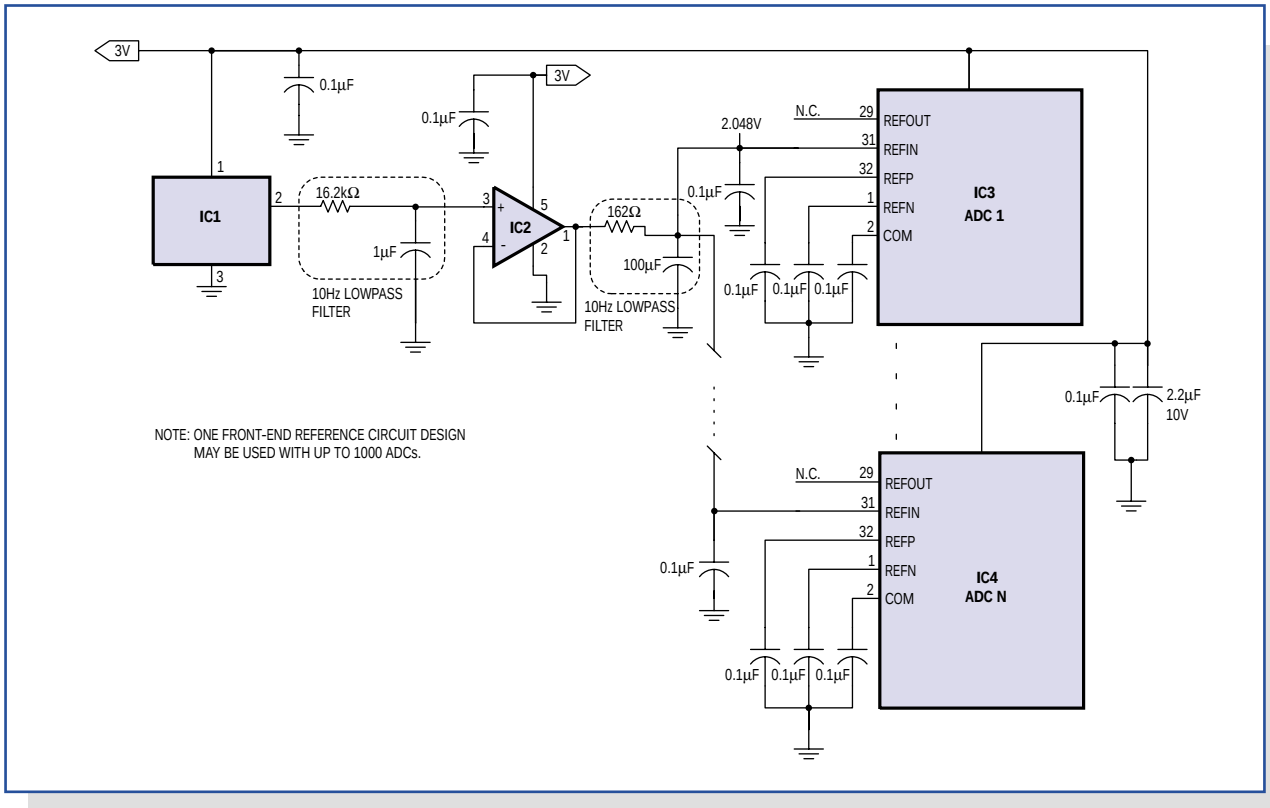


Figure 1. For ultrasound applications, a single, low-noise reference circuit drives up to 1000 ADCs.

Those three voltages are buffered by the quad op amp IC2, which is selected for its low noise and DC offset. The individual voltage followers are connected to 10Hz lowpass filters which filter both the reference-voltage noise and buffer-amplifier noise to a level of $3nV/\sqrt{Hz}$. The 2.0V and 1.0V reference voltages set the differential full-scale range of the associated ADCs at $2V_{P-P}$. The 2.0V and 1.0V buffers drive the ADCs' internal-ladder resistances between them: 4kΩ divided by the number of ADCs in the circuit. As an example, 32 ADCs will draw 8mA from those supplies—a load current well within the capability of IC2.

This configuration's gain accuracy can be good, depending on the accuracy grade of IC1 and the tolerance of resistors in the voltage divider. The gain matching of each ADC in this configuration is typically 0.1%. With the noise level below $3nV/\sqrt{Hz}$ at 100Hz, this circuit provides exemplary performance. As in Figure 1, the common power supply for all active components removes any concern about power-supply sequencing when powering up or down.

With the outputs of the op amp buffers matching better than 0.1%, the buffers and subsequent lowpass filters can be replicated to support as many as 32 ADCs. For applications that require more than 32 matched ADCs, a voltage reference and divider string common to all converters are highly recommended.

Conclusion

Systems requiring large numbers of data converters with good channel-to-channel matching require careful design of the voltage-reference system. The use of a common, high-precision, low-noise reference driving all the ADCs is a valuable approach for achieving high-accuracy matching. The flexible reference inputs and exceptional dynamic performance of 10-bit ADCs in the MAX144x family make them compelling candidates for such applications.

(A similar idea appeared in the 1/24/02 issue of *EDN*.)

References:

1. Maxim MAX1444 data sheet, Rev. 0, 10/00.
2. Maxim MAX1448EVKIT data sheet, Rev. 1, 12/01.
3. Maxim MAX4249–MAX4252 data sheet, Rev. 4, 1/02.
4. Maxim MAX6061–MAX6068 data sheet, Rev. 1, 5/01.

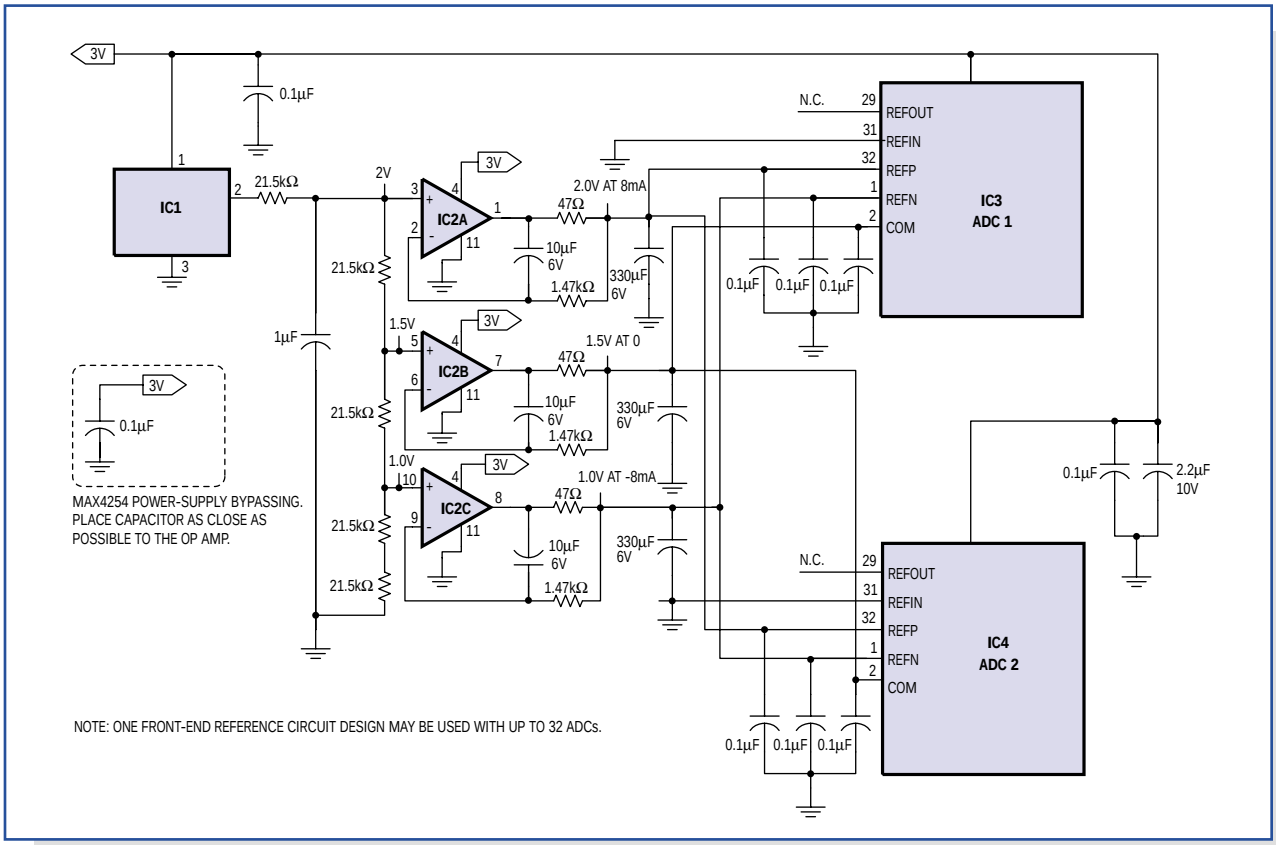


Figure 2. Also for ultrasound applications, a precision, low-noise reference circuit drives up to 32 ADCs.

Designing compact telecom power supplies

Telecom power supplies are specified for operation over a wide input-voltage range (36V to 75V) but with circuit performance optimized at 48V. Such circuit designs should be compact, efficient, and have a low profile to comply with the tight spacing between cards. This article discusses a 5W flyback converter for telecom applications, based on the MAX5021—a universal offline power-supply controller.

Telecom systems include numerous line cards. Connected in parallel to the high-power backplane, each has its own input-filter capacitor and low-voltage power converter. The large number of input-filter capacitors in parallel limits the value of each to a few microfarads, making the power-supply design fairly difficult.

The MAX5021 IC is a high-frequency, current-mode PWM controller suitable for wide-input-range, isolated telecom power supplies. It enables the design of small, efficient, power-converter circuits. A fixed-switching frequency of 262kHz controls switching losses while allowing moderately small power components. The IC includes undervoltage lockout capability with large hysteresis and a low startup current. This results in low-loss designs for power supplies that feature a wide input-voltage range and low output power. Cycle-by-cycle current limiting (achieved with a fast internal comparator) reduces overdesign in the MOSFET and transformer. Other features include maximum-duty-cycle limiting and high-peak capability for the source and sink-drive currents. A reference design **(Figure 1)** illustrates the 5W flyback converter with an input-voltage range of 36V to 72V.

Power-stage design

The first step in designing a power supply is deciding on a conversion topology. Topology selection criteria include the input-voltage range, output voltage, peak currents in the primary and secondary circuits, efficiency, form factor, and cost.

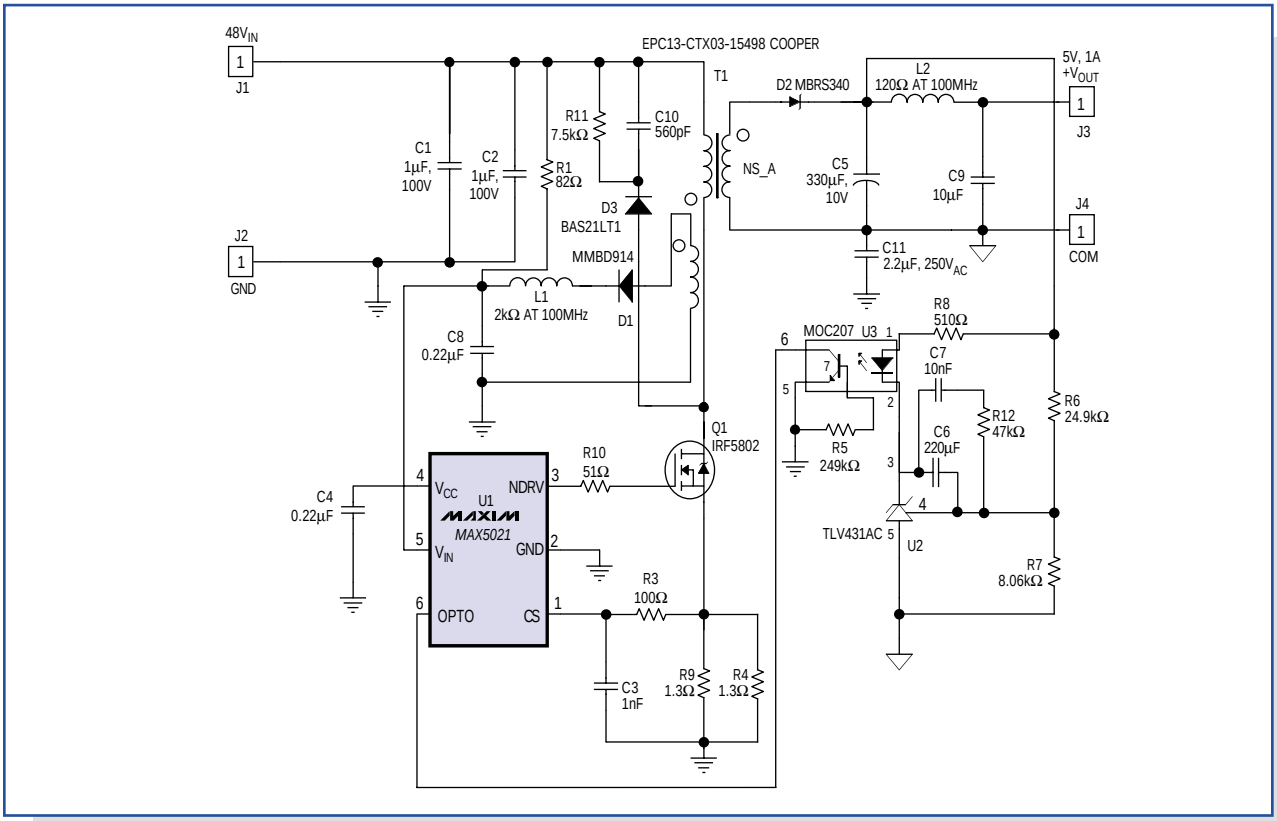


Figure 1. Based on the MAX5021 PWM controller, this flyback converter for telecom applications delivers 5W at 5V.

The best choice for a 5W output with a 1:2 input-voltage range and small form factor is a flyback topology whose minimum component count reduces the cost and form factor. The flyback transformer can be designed to operate either in continuous or discontinuous mode. Discontinuous mode causes the transformer core to complete its energy transfer during the off cycle, and continuous mode allows the next cycle to begin before the energy transfer is complete. In the present case, discontinuous mode is chosen for the following reasons: it maximizes energy storage in the magnetic component (thereby reducing the component's size); it simplifies compensation (no right-half-plane zero); and it yields a higher unity-gain bandwidth.

A disadvantage of the discontinuous operating mode is the higher ratio of peak-to-average current in the primary and secondary circuits. A higher ratio means higher RMS current, which leads to higher loss and lower efficiency. For low-power conversion, the advantages of discontinuous mode easily surpass the disadvantages. Moreover, the IC's drive capability is sufficient for driving the large switching MOSFET necessary to carry these peak currents. A telecom application using the MAX5021 in this topology easily achieves power outputs to 15W using standard MOSFETs.

Transformer design

The key to low loss and high efficiency in the transformer is a proper core. The core and the winding-area product determine the amount of power the transformer can handle with an acceptable rise in temperature. Also considered in the core selection are the topology (ratio of average to RMS current in the winding), output current, efficiency, and form factor. The design of a discontinuous-mode transformer is explained below, step by step. Note that the first equation is a general one, and the second is specific to the MAX5021 power supply with a 40°C temperature rise.

- Estimate the minimum area-product requirement, and select a core and bobbin with suitable form factor.
- Calculate the secondary-winding inductance for guaranteed core discharge within the minimum off-time.
- Calculate the primary-winding inductance for sufficient energy to support maximum load.
- Calculate the number of turns in the primary.
- Calculate the number of turns in the secondary and bias windings.
- Calculate the A_L value of the core.
- Calculate the RMS current in the primary, and estimate the secondary RMS current.
- Consider the proper winding sequence and transformer construction for low leakage.

1) Use the following equation to estimate the minimum area product required:

$$A_P \geq \frac{(1.1 \times P_{OUT} \times D_{MAX})}{\eta \times K_P \times K_U \times J \times K_T \times B_{MAX} \times f_{SW(MIN)}} ...(m^4)$$

$$A_P \geq \frac{(2 \times P_{OUT}) \times 10^{-12}}{\eta \times B_{MAX}} ...(m^4)$$

where:

η = expected efficiency of the converter;

K_P = area assigned to the primary (usually 0.5);

K_T = ratio of RMS to average current in the primary (0.55 to 0.65 for discontinuous flyback);

K_U = window utilization factor (0.4 to 0.5);

J = current density ($9.862 \times 10^6 A/m^2$ for winding temperature rise less than 40°C); and

B_{MAX} = maximum operating flux density in Teslas (use between 0.12T to 0.15T).

Select a core with area product (A_P) equal to or greater than the figure calculated above, and note its core cross section area. Refer to the following table for output power vs. core size, A_P, and core cross-section area (A_e):

Output Power vs. Core Size

Output Power (W)	Core Size	A_p (mm^4)	A_e (mm^2)
Up to 2	EPC-10	30	9.4
3 to 4	EEM-12.7	90	12
5 to 8	EPC-13	145	12.5
9 to 12	EPD-15	216	13.5

(Refer to the Appendix on page 13 for an example.)

2) As discussed earlier, discontinuous operation requires that the core be discharged during the off-cycle. Secondary inductance determines the time required to discharge the core. Use the following equations to calculate secondary inductance:

$$L_S \leq \frac{(V_O + V_D) \times (D_{OFF(MIN)})^2}{2 \times I_{OUT} \times f_{SW(MAX)}} ...(H)$$

$$L_S \leq \frac{430 \times 10^{-9} \times (V_O + V_D)}{I_{OUT}} ...(H)$$

where:
V_D = secondary-diode forward-voltage drop in volts.
I_{OUT} = maximum-rated output current in amperes.

3) Rising current in the primary builds energy in the core during the on-cycle, which is then released to deliver output power during the off-cycle. The primary inductance must hold enough energy during the on-time to support the maximum output power.

$$L_P = \frac{V_{IN(MIN)}^2 \times D_{MAX}^2 \times \eta}{2 \times P_{OUT} \times f_{S(MAX)}}$$

$$L_P = \frac{0.4 \times 10^{-6} \times V_{IN(MIN)}^2 \times \eta}{P_{OUT}} ...(H)$$

4) Next, calculate the primary number of turns necessary to keep the maximum flux density within limits at the maximum V-s product across the primary. The maximum-operating peak current occurs at the maximum duty cycle.

$$N_P = \frac{V_{IN(MIN)} \times D_{MAX}}{A_e \times B_{MAX} \times f_{S(MIN)}} ...(Turns)$$

$$N_P = \frac{2.1 \times 10^{-6} \times V_{IN(MIN)}}{A_e \times B_{MAX}} ...(Turns)$$

where:
A_e = core cross section area in square meters.

5) Round off the primary number of turns to the closest integer, and calculate the number of turns for the secondary and bias windings using the rounded-off primary number of turns. Refer to the following equation:

$$N_S = N_P \times \sqrt{\frac{L_S}{L_P}} ...(Turns)$$

$$N_{BIAS} = \frac{11.7}{V_{OUT} + 0.2} ...(Turns)$$

The forward-bias drops of secondary- and bias-rectifier diodes are assumed to be 0.2V and 0.7V, respectively. Refer to the diode manufacturer's data sheet to verify these numbers. Again, round off the number of turns for secondary and bias windings to the closest integers.

6) The core's A_L value depends on the air gap in the magnetic path length. Most of the energy is stored in the air gap during the MOSFET's on time. To reduce electromagnetic radiation, insert the air gap in the center leg of the core.

$$A_L = \frac{L_P}{N_P^2} \times 10^9 ... \frac{nH}{Turns^2}$$

7) The transformer manufacturer must know the RMS currents in the primary, secondary, and bias windings to decide the thickness of the wire. To keep skin-effect loss under control, only wires thinner than 28AWG are recommended. Multiple wires in parallel can be used to achieve the required copper thickness. Multifilar windings are very common in high-frequency converters. Maximum RMS current in the primary and secondary windings occurs at 50% duty cycles (minimum input voltage) and maximum output power. Use the following equations to calculate primary and secondary RMS currents:

$$I_{PRMS} = \frac{P_{OUT}}{0.5 \times D_{MAX} \times \eta \times V_{IN(MIN)}} \times \sqrt{\frac{D_{MAX}}{3}} ...(A)$$

$$I_{PRMS} = \frac{1.63 \times P_{OUT}}{\eta \times V_{IN(MIN)}} ...(A)$$

$$I_{SRMS} = \frac{I_{OUT}}{0.5 \times D_{OFF(MAX)}} \sqrt{\frac{D_{OFF(MAX)}}{3}} ...(A)$$

$$I_{SRMS} = 1.63 \times I_{OUT} .....(A)$$

Bias current is usually less than 10mA, so the selection of wire thickness depends more on the convenience of winding the wire than its current capacity.

8) The winding technique and sequencing is important in achieving a lower leakage-inductance spike at switch turn-off. As an example, interleave the secondary between two primary halves and keep the bias winding close to the secondary, so the bias voltage follows the output voltage.

MOSFET selection

Selection criteria for the MOSFET include maximum drain voltage, peak/RMS current in the primary, and maximum-allowable power dissipation for the package (without exceeding the junction temperature limits). Voltage at the MOSFET drain is the sum of the input voltage, the secondary voltage reflected through the transformer turns ratio, and the leakage-inductance spike. (**Figure 2** illustrates the relationship between drain voltage and primary current.) The MOSFET's absolute maximum V_{DS} rating must be higher than the worst-case drain voltage (maximum input voltage and output load).

$$V_{DS(MAX)} = V_{IN(MAX)} + \frac{N_P}{N_S} \times (V_{OUT} + V_D) + V_{SPIKE} ...(V)$$

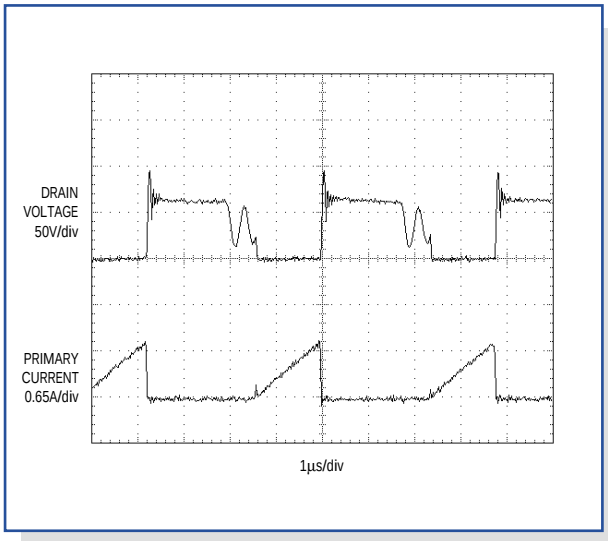


Figure 2. This scope photo shows Figure 1's circuit operating at V_{IN} = 36V, V_{OUT} = 5V, and I_{OUT} = 1A. The switching MOSFET (Q1) exhibits drain voltage (upper trace) at 50V/div, and primary current (lower trace) at 0.65A/div.

A lower V_{DS} Absolute Maximum Rating means a shorter channel, lower $R_{DS(ON)}$, lower gate charge, and a smaller package. Thus, it is advisable to keep $V_{DS(MAX)}$ low by choosing a lower N_P/N_S ratio and keeping the leakage-inductance spike under control. A resistor/capacitor/diode (RCD) snubber network can suppress such spikes.

The RMS current in the primary can be used to calculate DC loss in the MOSFET. Switching loss in the MOSFET depends on the operating frequency, the total gate charge, and the cross-conduction loss during turn-off. Cross-conduction loss during turn-on is negligible, because in discontinuous-conduction mode the primary current starts from zero. To avoid damage during power-on and during fault conditions, it may be necessary to derate the MOSFET. Use the following equation to estimate the MOSFET's power dissipation:

$$P_{MOS} = (1.4 \times R_{DS(ON)} \times I_{PRMS}) + (Q_G \times V_{CC} \times f_{S(MAX)}) + \frac{(V_{IN(MAX)} \times I_{PK} \times t_{off} \times f_{S(MAX)})}{4} + \frac{(C_{DS} \times V_{DS}^2 \times f_{S(MAX)})}{2} ...(W)$$

where:

Q_G = total gate charge of the MOSFET in coulombs;

V_{CC} = bias voltage in volts;

t_{OFF} = turn-off time in seconds;

C_{DS} = drain-to-source capacitance in farads.

RCD snubber-network design

To avoid an excessive V_{DS} requirement for the MOSFET, we recommend using an RCD snubber across the primary to suppress the spike caused by energy in the leakage inductance. The snubber dissipates energy that would otherwise dissipate in the MOSFET itself. The snubber capacitor's value should be high enough to absorb the leakage-inductance energy without allowing the MOSFET drain voltage to rise beyond an acceptable limit. Use the following equation to calculate this capacitance:

$$C = \frac{L_L \times I_{PK}^2}{V_{SPIKE}^2} ...(F)$$

where:

L_L = leakage inductance, which should be specified by the transformer vendor. (Values of 1µH to 3µH are common for the transformer under discussion.) V_{SPIKE} = spike voltage, typically 30V to 50V. I_{PK} = peak primary current, which in this case (for a worst-case spike) equals the current-limit threshold divided by R_{SENSE}.

The diode must be a fast-switching type, with reverse-blocking voltage at least equal to the $V_{DS(MAX)}$ rating of the MOSFET. The resistor is selected for an RC time constant 2 to 3 times the switching period. Power dissipation in the resistor is the sum of the leakage-inductance energy times frequency, plus the power loss caused by DC bias across the capacitor. The following equation lets you estimate power dissipation in the resistor:

$$P_R = (\frac{1}{2} \times C_{SNUBBER} \times V_{SPIKE}^2) f_{S(MAX)} + \frac{[(V_O + V_D) \times \frac{N_P}{N_S}]^2 \times (1 - D_{MIN})}{R_{SNUBBER}}$$

where:

D_{MIN} = minimum duty cycle = $D_{MAX}/2$. (A 50% derating is recommended for chip resistors.)

Input filter design

The input filter reduces the amplitude of AC components in the converter's current pulses, thereby making the converter appear to the source as a DC load. Design parameters for this filter are the RMS ripple-current capability, input voltage, and the allowable level for AC components reflected back to the source.

Because discontinuous-mode flyback converters draw peak triangular currents through the capacitor ESR during each cycle, large aluminum electrolytic capacitors are needed for their low ESR and high ripple-current ratings. Unfortunately for a distributed power system, the input-filter capacitances of parallel converters add

together and may produce an unacceptable inrush current at startup. As an alternative, you can use ceramic capacitors to achieve low ESR and a high ripple-current rating while keeping the total capacitance low.

The input peak-to-peak ripple voltage is a combination of the voltage drop due to capacitor ESR (ΔV_{ESR}) and the loss of charge from the capacitor (ΔV_C). For low-ESR ceramic capacitors, use a 3:1 contribution from charge loss and ESR ripple respectively, and use the following equation to estimate capacitance and ESR for the capacitor:

$$C_{IN} = \frac{4 \times P_{OUT} \times 10^{-6}}{\eta \times V_{IN(MIN)} \times \Delta V_C} ...(F)$$

And,

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{PK}} ....(\Omega)$$

Choose a capacitor that can handle the necessary RMS ripple without increasing its internal temperature **(Figure 3)**. Use the following equation to estimate RMS ripple in the input capacitor:

$$I_{CRMS} = \frac{1.63 \times P_{OUT}}{\eta \times V_{IN(MIN)}} ...(A)$$

Output filter design

The output capacitance required depends on the level of peak-to-peak ripple acceptable at the load end. The output capacitor for flyback converters supports load current during the switch on-time. The transformer secondary replenishes those lost charges by discharging the core during the off-cycle, and simultaneously supplies the load current. Again, output ripple is the sum of the voltage drop due to the output capacitor's ESR (ΔV_{ESR}), and the charge loss (ΔV_C) during the switch on-time. High switching frequency in the MAX5021 reduces the capacitance requirement. Use low-ESR tantalum capacitors for their favorable combination of capacitance and ESR, and use the following equations to calculate the capacitance and ESR:

$$C_{OUT} = \frac{4 \times (1 - D_{OFF}) \times I_O \times 10^{-6}}{\Delta V_C} ...(F)$$

And,

$$ESR_O = \frac{\Delta V_{ESR}}{I_O} ...(\Omega)$$

where:

D_{OFF} is the discharge duty cycle, calculated using the following equation:

$$D_{OFF} = \sqrt{\frac{I_O \times L_S}{2 \times 10^{-6} \times (V_O + V_D)}}$$

Additional noise spikes ride on the output ripple, caused by the di/dt of secondary current flowing through the output capacitor's ESL. A small LC filter can suppress these low-energy spikes, and it helps in attenuating switching-frequency ripple as well. To minimize the filter's effect on phase loss and to ensure that it does not interfere with compensation, you should design its corner frequency more than one decade away from the estimated closed-loop bandwidth. **Figure 4** shows the peak-to-peak ripple waveforms with and without the LC filter. Use a low-ESR ceramic capacitor of 1µF to 10µF, and calculate the inductance using the following equation:

$$L \le \frac{1}{4 \times 10^3 \times f_C^2 \times C} ...(H)$$

where:

f_C = estimated closed-loop bandwidth.

Power loss consideration

High-frequency switching converters can be very lossy, since switching loss simply adds to the DC loss. Careful component selection is necessary to keep switching loss at a minimum. The MAX5021 is designed to operate at a sufficiently high frequency to reduce the size of passive components while minimizing switching losses. The MAX5021's low startup current and low quiescent operating current minimize power loss in the control circuitry. To reduce switching loss even further and achieve higher converter efficiency, use a MOSFET with

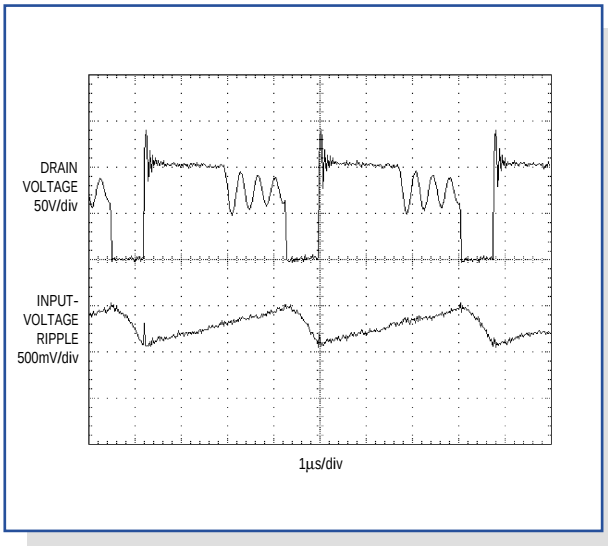


Figure 3. This scope photo shows Figure 1's circuit operating at V_{IN} = 72V, V_{OUT} = 5V, and I_{OUT} = 1A. The circuit exhibits input-voltage ripple at 500mV/div (lower trace) and drain voltage at 50V/div (upper trace).

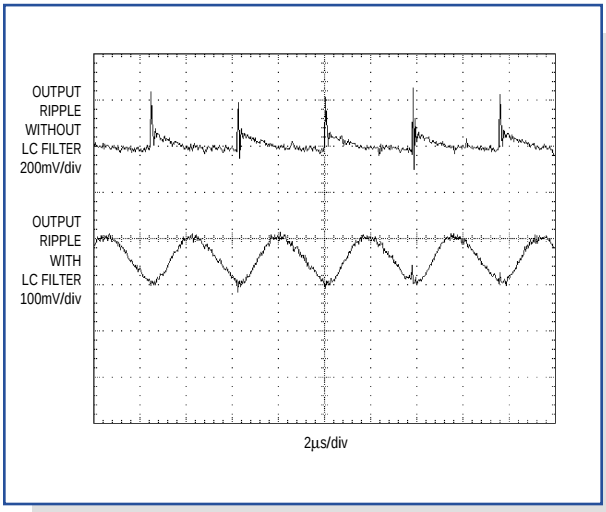


Figure 4. This scope photo shows Figure 1's circuit operating at V_{IN} = 72V, V_{OUT} = 5V, and I_{OUT} = 1A. The circuit has less output-voltage ripple with an LC filter (lower trace at 100mV/div) than without (upper trace at 200mV/div).

low gate charge and low gate-to-drain capacitance, and balance the MOSFET's DC and switching-power losses. See graph of Converter Efficiency vs. Output Current **(Figure 5)**, and use the following equation to calculate DC and switching losses in the MOSFET:

$$P_{MOS} = (1.4R_{DS(ON)} \times I_{PRMS}) + (Q_G \times f_{SW} \times V_{CC}) + \left(\frac{I_{PK} \times V_D \times t_F \times f_{SW}}{6}\right)$$

where:
Q_G = total gate charge for the MOSFET in nanocoulombs;
V_{CC} = voltage at V_{CC} (pin 4 of MAX5021);

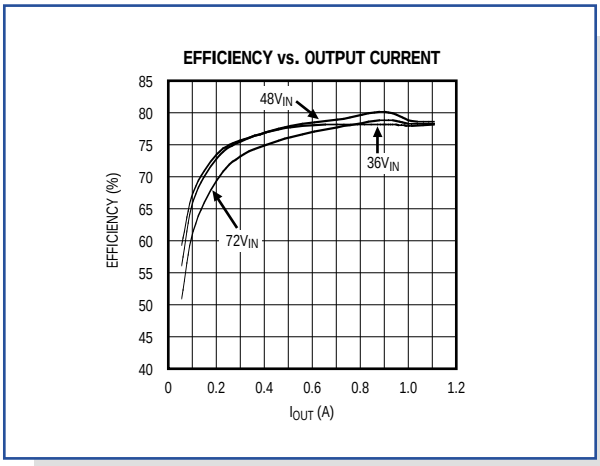


Figure 5. This graph demonstrates Efficiency vs. Output Current curves for the circuit in Figure 1.

t_F = turn-off time in seconds;
V_D = drain voltage at turn-off in volts;
f_{SW} = switching frequency (262kHz);
I_{PK} = primary peak current in amperes.

Use a Schottky diode in the secondary to achieve low V_{DS} and low reverse-recovery loss. Use the following equation to calculate DC loss in the secondary diode while neglecting reverse-recovery loss due to switching:

$$P_D = V_{FB} \times I_O$$

where:
V_{FB} = forward drop for the secondary diode at $I_{SPK}/2$, in volts.

You can reduce the transformer-leakage inductance between primary and secondary by sandwiching the secondary between two halves of the primary. Use a multifilar winding structure to reduce skin-effect loss.

Frequency compensation

The absence of a right-half-plane (RHP) zero in the discontinuous flyback converter simplifies the closed-loop frequency compensation to a single pole-zero pair. No bandwidth limit arises from the location of the RHP zero. The loop is closed through the shunt regulator, optocoupler, and PWM comparator internal to the MAX5021. The location of the error amplifier's pole and zero is determined from the existing PWM gain, the output-filter pole, and the ESR zero frequency. Use the following equations to calculate the current-mode converter's PWM gain, the output-capacitor filter pole, and the output capacitor's ESR zero:

$$A_{PWM} = \frac{\sqrt{\frac{R_L \times L_P \times f_{SW} \times \eta}{2}}}{R_S} \times \frac{6.2 \times 10^3}{R_{LED}} \times CTR$$

$$A_{PWM} = \frac{\sqrt{\frac{5 \times 61 \times 10^{-6} \times 262 \times 10^3 \times 0.8}{2}}}{0.65} \times \frac{6.2 \times 10^3}{510} \times 1$$

$$A_{PWM} = 105$$

Capacitor filter pole (f_P):

$$f_P = \frac{1}{2 \times \pi \times R_L \times C_O} ...(Hz)$$

$$f_P = \frac{1}{2 \times \pi \times 5 \times 330 \times 10^{-6}} ...(Hz)$$

$$f_P = 96...(Hz)$$

Capacitor ESR zero (f_z):

$$f_z = \frac{1}{2 \times \pi \times C_O \times ESR} ...(Hz)$$

$$f_z = \frac{1}{2 \times \pi \times 330 \times 10^{-6} \times 0.06} ....(Hz)$$

$$f_z = 8038....(Hz)$$

where:

R_L = load resistance;

CTR = current-transfer ratio of optocoupler;

R_S = current-sense resistor in the primary path; and

C_O = output-filter capacitor.

Total loop gain equals the PWM gain (A_{PWM}) times the gain of the voltage divider and the error amplifier (shunt regulator). The available worst-case phase margin (PM) occurs at full load.

The response of the combined-error amplifier, optocoupler, and PWM is too complicated to estimate analytically. You should therefore use the existing compensation network to plot a Bode diagram of the closed-loop transfer function from control to output. Then place the zero and pole at appropriate locations for maximum "phase bump" at the crossover frequency. To maintain a gain slope of -1 to well beyond the crossover frequency, place the error-amplifier pole at the ESR zero location. Use the following equations to calculate the zero (f_{ZE}) and poles (f_{PE}) of the error amplifier:

$$f_{ZE} = \frac{1}{2 \times \pi \times R_f \times C_f} ...(Hz)$$

$$f_{ZE} = \frac{1}{2 \times \pi \times 47 \times 10^3 \times 10 \times 10^{-9}} ...(Hz)$$

$$f_{ZE} = 338...(Hz)$$

$$f_{PE} = \frac{1}{2 \times \pi \times R_f \times C_{ff}} ....(Hz)$$

$$f_{PE} = \frac{1}{2 \times \pi \times 47 \times 10^3 \times 220 \times 10^{-12}} ....(Hz)$$

$$f_{PE} = 15,392....(Hz)$$

Optimization on the board produces a closed-loop bandwidth of 8kHz with 44° of phase margin. The Bode plot of **Figure 6** is based on the circuit of Figure 1, with values as shown for the compensation components.

We can verify the load-transient response for a small-deviation, fast-settling perturbation in the output voltage by switching the load from 100mA to 1A in 20µs **(Figure 7)**. An overcompensated converter increases the response time, which may also cause an output overshoot during turn-on. **Figure 8** depicts the result of an optimally compensated loop.

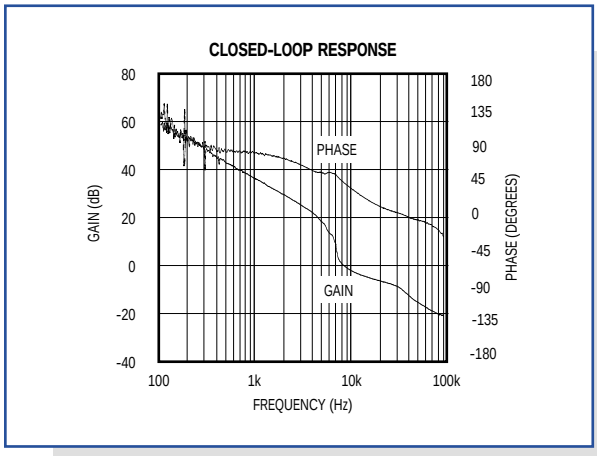


Figure 6. This Bode plot illustrates stability for Figure 1's circuit operating with component values as shown.

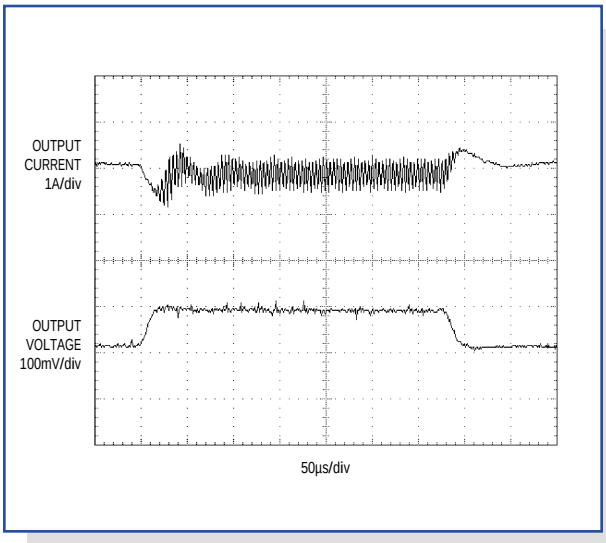


Figure 7. The transient response for Figure 1's circuit: I_{OUT} at 1A/div (lower trace), and V_{OUT} at 100mV/div (upper trace).

Layout and safety guidelines

High-frequency switching converters produce current and voltage waveforms with high slew rates. To minimize voltage spikes and electromagnetic radiation, you should minimize inductance in the current loops and PC traces. Component placement is critical in keeping the high-frequency traces short. Follow the steps below for good layout:

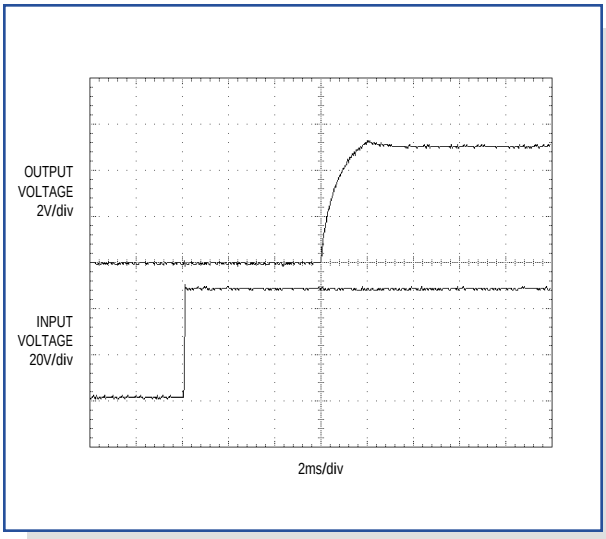


Figure 8. These startup waveforms appear in Figure 1's circuit with an optimally compensated loop. The circuit has a 48V input voltage at 20V/div (lower trace), and a 5V output voltage with 1A load at 2V/div (upper trace).

- Minimize the loop formed by the input capacitor positive terminal, transformer primary, MOSFET switch, current-sense resistor, and input-capacitor negative terminal.
- Keep the gate-drive trace from the MAX5021 to the switching MOSFET short.
- Place the RCD snubber components close to the input capacitor and MOSFET switch.
- Place the ceramic capacitors connected to the MAX5021 V_{CC}, V_{IN}, and CS pins close to the IC.
- Minimize the loop formed by the transformer secondary, secondary diode, and output capacitor.
- For effective heatsinking on the PC board, connect a large copper area to the MOSFET drain, transformer secondary, and secondary diode.

The type of circuit (SELV, TNV-1, TNV-2, or TNV-3) and its degree of pollution (determined by the circuit surroundings) determine the requirements for clearance and creepage between the primary and secondary circuits. For the minimum clearance and creepage distances between different circuit components, contact your safety engineer or refer to Underwriters Laboratory standard UL60950.

Appendix—Transformer Design

Given the specifications V_{IN} = 36V to 72V, V_{OUT} = 5.1V, and I_{OUT} = 1.1A, proceed as follows:

Step 1. Area product (A_P):

$$A_p \geq \frac{(2 \times P_{OUT}) \times 10^{-12}}{\eta \times B_{MAX}} ...(m^4)$$

$$A_p \geq \frac{(2 \times 5.61) \times 10^{-12}}{0.8 \times 0.12} ...(m^4)$$

$$A_p \geq 117 \times 10^{-12} ....(m^4)$$

Select EPC13 (TDK Part Number – PC44EPC13-Z) Core A_p and A_e:

$$A_p = 145 \times 10^{-12} ....(m^4)$$

$$A_e = 12.5 \times 10^{-6} ....(m^2)$$

Step 2. Secondary inductance (L_S):

$$L_S \leq \frac{430 \times 10^{-9} \times (V_O + V_D)}{I_{OUT}} ...(H)$$

$$L_S \leq \frac{430 \times 10^{-9} \times (5.1 + 0.4)}{1.1} ...(H)$$

$$L_S \leq 2.15 \times 10^{-6} ...(H)$$

Step 3. Primary inductance (L_P):

$$L_P = \frac{0.4 \times 10^{-6} \times V_{IN(MIN)}^2 \times \eta}{P_{OUT}} ...(H)$$

$$L_P = \frac{0.4 \times 10^{-6} \times 34^2 \times 0.8}{5.6} ...(H)$$

$$L_P = 65 \times 10^{-6} ....(H)$$

Step 4. Primary turns (N_P):

$$N_P = \frac{2.1 \times 10^{-6} \times V_{IN(MIN)}}{A_e \times B_{MAX}} ...(Turns)$$

$$N_P = \frac{2.1 \times 10^{-6} \times 36}{12.5 \times 10^{-6} \times 0.12} ...(Turns)$$

$$N_P = 47.6 ...(Turns)$$

Round off the primary turns, N_P = 48.

Step 5. Secondary- and bias-winding turns (N_S and N_{bias}):

$$N_S = N_P \times \sqrt{\frac{L_S}{L_P}} \text{ ...(Turns)}$$

$$N_S = 8.7 \text{ ...(Turns)}$$

Round off the secondary turns, $N_S = 9$:

$$N_{bias} = \frac{11.7}{V_{OUT} + 0.2} \times N_S$$

$$N_{bias} = 19.8$$

Round off the bias-winding turns, $N_{bias} = 20$.

Step 6. Value of the core:

$$A_L = \frac{L_P}{N_P{}^2} \times 10^9 \ldots \frac{nH}{Turns^2}$$

$$A_L = 26 \ldots \frac{nH}{Turns^2}$$

Step 7. Primary and secondary RMS currents (I_{PRMS} and I_{SRMS}):

$$I_{PRMS} = \frac{1.63 \times P_{OUT}}{\eta \times V_{IN\,MIN}} \text{....(A)}$$

$$I_{PRMS} = \frac{1.63 \times 5.1 \times 1.1}{0.8 \times 34} \text{....(A)}$$

$$I_{PRMS} = 0.33 \text{....(A)}$$

$$I_{SRMS} = 1.63 \times I_{OUT} \text{....(A)}$$

$$I_{SRMS} = 1.79 \text{....(A)}$$

Small, high-voltage boost converters

The biasing of avalanche photodiodes (APDs), piezoelectric transducers (PZTs), vacuum fluorescent displays (VFDs), and microelectromechanical systems (MEMS) require high-voltage power supplies. This article presents three topologies ***(Figures 1a, 1b,*** *and* ***1c)*** *for generating a high output voltage from a low input voltage. The advantages and disadvantages of each are discussed with focus given to power density and circuit size. The end of the article presents experimental data to contrast transformer-based and inductor-based solutions.*

The high-voltage bias required in many APD applications (75V) is derived from a 3V supply. That requirement presents the following challenges:

- High-voltage MOSFETs generally do not operate with a low 3V gate drive.
- The larger drain-source capacitance of high-voltage MOSFETs requires energy in the inductor to slew the drain to the output voltage. The resulting losses are as large as $^1/_2\ f_{switch} \times C_{DS} V_{OUT}^2$.
- High-voltage MOSFETs are larger and more expensive than their lower voltage counterparts. High-voltage power MOSFETs are seldom found within switching-controller ICs.
- Extreme duty cycles impose inefficiently small off-times or low switching frequencies. Lower switching frequency causes higher ripple and requires larger magnetics.

The circuit of Figure 1c solves these challenges by using an autotransformer. The peak voltage on the MOSFET is reduced, allowing the use of the MAX1605, which has a 28V internal MOSFET. The complete layout (smaller than an 8-pin DIP) fits on a 6mm x 8.5mm double-sided board **(Figure 2)**.

Theory of operation

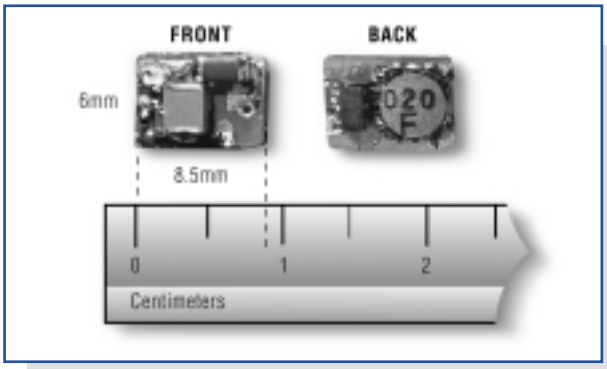
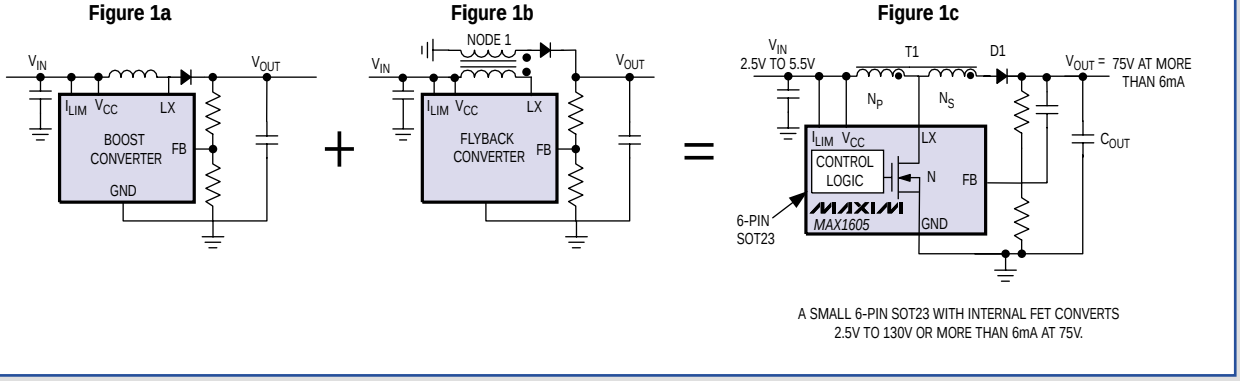


Figure 2. This 6mm x 8.5mm DC-DC converter converts 2.5V to 75V using the MAX1605. The front and back layout of the circuit is shown.

Standard boost and flyback DC-DC converters can be merged to form the hybrid topology of Figure 1c. The resulting merged topology stacks secondary-winding flyback voltage on top of the input voltage and the primary-winding flyback voltage (a standard flyback converter only takes advantage of flyback voltage produced at the secondary side). Compared with a standard boost converter, this topology produces higher output voltages from a lower voltage MOSFET by limiting the voltage seen at LX.

A transformer provides the following advantages:

- Higher attainable output voltages;
- Lower operating duty cycle;
- Lower voltage on the MOSFET.



Figures 1a, 1b, and 1c. These high-voltage DC-DC converters in three topologies are used to create high output voltage from low input voltage.

The following advantages also accrue when operating the transformer in discontinuous mode, with a constant peak current in the MOSFET:

- Higher switching frequency produces lower output ripple
- Higher frequency ripple
- Smaller magnetics

The MAX1605 and many other boost converters can be used in this topology. Maximum output voltage is limited by the transformer turns ratio, the transformer and diode voltage ratings, the MOSFET's voltage rating and drain capacitance, and the diode's reverse-recovery time.

Standard boost

The standard boost converter is shown in Figure 1a. When the MOSFET turns on, the inductor current ramps up. When the MOSFET turns off, LX flies up to V_{OUT} + V_D, and the inductor current ramps down. Intuitively, if the inductor spends 1/nth of its time delivering energy to the output, the output voltage (V_{OUT}) is n times the input voltage (V_{IN}), thus the following equation can be generated:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D}$$

where D is the duty cycle. A more analytical proof can be found by using **Figure 3**. The key to this proof lies in steady-state operation, for which the current must ramp down the same amount that it ramps up:

$$\Delta I_{UP} = \Delta I_{DOWN}$$

Thus, the final inductor current equals the initial inductor current.

$$\Delta I_{UP} = \frac{V_{IN}}{L_{BST}} t_{ON} = \frac{V_{IN}}{L_{BST}} D \times T$$

$$\Delta I_{DOWN} = \frac{V_{OUT} - V_{IN}}{L_{BST}} t_{OFF} = \frac{V_{OUT} - V_{IN}}{L_{BST}} (1-D) \times T$$

Because they are equal,

$$\frac{V_{IN}}{L_{BST}} D \times T = \frac{V_{OUT} - V_{IN}}{L_{BST}} (1-D) \times T$$

$$V_{IN} \times D = V_{OUT} - V_{IN} \times (1-D)$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{(1-D)} \quad \text{and} \quad D = 1 - \frac{V_{IN}}{V_{OUT}}$$

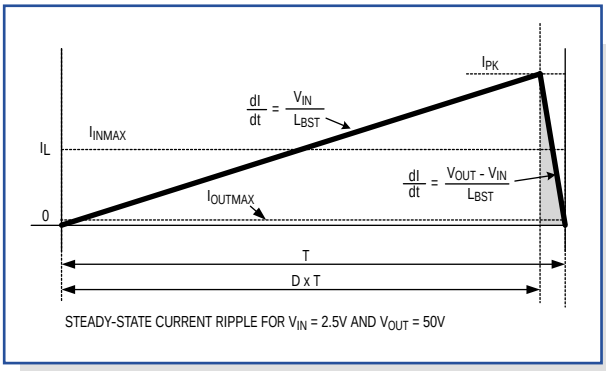


Figure 3. This analysis of the inductor current for the circuit of Figure 1a can be used to determine its duty cycle.

The circuit of Figure 1b could be made equivalent to the circuit of Figure 1a by connecting the left side of the transformer's secondary winding to V_{IN} and setting the turns ratio to 1. The secondary-side diode can be reflected to the primary side, making the relationship between a flyback converter and a boost converter easier to perceive.

Turns ratios larger than 1:1 provide leverage by allowing higher output voltage with less extreme duty cycles. Alternatively, node 1 of the transformer can be connected to any power supply, enabling leverage with respect to that supply. Because LX flies up during the off-cycle, an additional voltage step can be obtained by connecting node 1 to LX, as shown in Figure 1c. That connection also helps catch some of the leakage energy that would otherwise be dumped from the transformer's primary side to the MOSFET, producing short, high-voltage spikes at the MOSFET's drain. If the voltage spikes are higher than the MOSFET's voltage tolerance, a snubber circuit will be necessary to dissipate the leakage energy.

LX is shorted to ground in Figure 1b, allowing the primary-side current to ramp up as for an inductor. No current flows through the secondary side of the transformer and the diode is reverse-biased because

$$V_{PRIMARY} = -V_{IN}$$
$$V_{SECONDARY} = N_S / N_P \times V_{PRIMARY}$$

Primary-side current must cease when the switch at LX turns off, but the N x I product must remain constant:

$$I_{P\_initial} \times N_P + I_{S\_initial} \times N_S = I_{P\_final} \times N_P + I_{S\_final} \times N_S$$

where subscript "P" indicates primary side, subscript "S" indicates secondary side, "initial" indicates current at the moment before the MOSFET is switched off, and "final" indicates current at the moment after the MOSFET is switched off.

Because $I_{S\_initial} = I_{P\_final} = 0$,

$$I_{S\_final} = \frac{N_P}{N_S} I_{P\_initial}$$

The circuit of Figure 1c is similar, except that $I_{P\_final} = I_{S\_final}$, thus

$$I_{S\_final} = \frac{N_P}{N_P + N_S} I_{P\_initial}$$

To simplify, the turns ratio 'N' is expressed as:

$$N = \frac{N_P + N_S}{N_P}$$

because the secondary side of Figure 1c never acts independently. Though unconventional, this definition for N is more appropriate for Figure 1c.

Figure 4 shows the primary-side current waveform for Figure 1c. For step-up converters whose output is more than twice the input voltage, off-time has a greater effect on the efficiency than on-time. Assume (for a comparable boost converter) that off-time has been minimized by minimizing inductance (L_{BST}), which also minimizes component size to the point that further reduction would lead to undesired efficiency loss. Then, select the Figure 4 transformer's total inductance to be N times as large. Because the primary-side current ramps down from I_{PK}/N instead of I_{PK}, the primary inductance must be N times as large to maintain the same off-time.

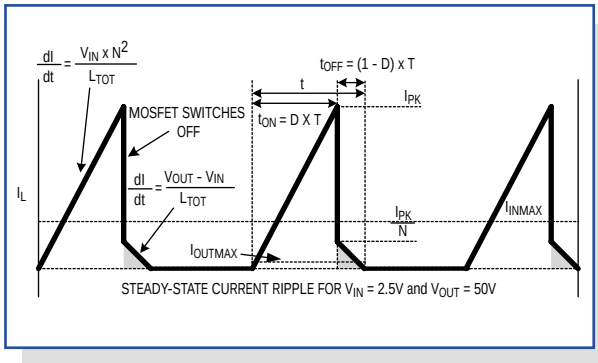


Figure 4. This analysis of the primary-side transformer current for the circuit of Figure 1c can be used to determine its duty cycle.

The primary-side inductance is:

$$L_P = \frac{L_{TOT}}{N^2}$$

where L_{TOT} is the total inductance of the autotransformer since L_P is N^2 smaller than L_{TOT}, and L_{TOT} is N times larger than L_{BST}, L_P is L_{BST}/N. As a result, the primary side ramps faster than a simple boost converter.

$$I_{SAT} = I_{PK} / N$$

$$L_{TOT} = L_{BST} \times N$$

$$L_P = L_{TOT} / N^2 = L_{BST} / N$$

For the steady state, it is clear from Figure 4 that:

$$\Delta I_{UP} = I_{PK} \quad \text{and} \quad \Delta I_{DOWN} = \frac{I_{PK}}{N} = \frac{\Delta I_{UP}}{N}$$

where ΔI_{UP} is the upward step in the primary-side current and ΔI_{DOWN} is the downward step. ΔI_{UP} and ΔI_{DOWN} can be calculated as follows:

$$\Delta I_{UP} = \frac{V_{IN}}{L_P} t_{ON} = \frac{V_{IN}}{L_{BST} / N} D \times T$$

and

$$\Delta I_{DOWN} = \frac{V_{OUT} - V_{IN}}{L_{TOT}} t_{OFF} = \frac{V_{OUT} - V_{IN}}{L_{BST} \times N} (1 - D) \times T$$

so

$$\frac{V_{OUT} - V_{IN}}{L_{BST} \times N} (1 - D) \times T = \frac{V_{IN}}{L_{BST} \times N / N} D \times T$$

Solving for V_{OUT}/V_{IN} yields:

$$\frac{V_{OUT}}{V_{IN}} = \frac{N \times D}{1 - D} + 1 \quad \text{and} \quad D = \frac{V_{OUT} - V_{IN}}{V_{IN}(N - 1) + V_{OUT}}$$

Figures 3 and 4 are both drawn to scale and have the same off-time (set to some optimal minimum). The shaded regions in Figures 3 and 4 represent energy delivered to the load, and the energy per pulse is proportional to the area of those regions. That energy can also be calculated from the expression $^1/_2 L \times I^2$ (note that L in Figure 4 is N times larger, and I is N times smaller). Because the circuit of Figure 1c delivers less energy per pulse, the ripple is N times smaller. Thus, a transformer not only leverages the output voltage up; it also leverages the output ripple down.

The topology of Figure 1c delivers less energy per pulse, but compensates by delivering more pulses, as clearly indicated in Figure 4. Figure 1c requires an N times larger inductance, but the saturation current can be N times smaller because the primary and secondary side see only I_{PK}/N as much current simultaneously. With an I_{SAT} smaller by a factor of N and an inductance N times larger, the transformer's energy-storage capability may also be N times smaller. Transformer size is a function of its energy-storage capability, so in theory you can use a transformer that is physically smaller by a factor of N. (In practice, the attainable size is determined by market limitations.)

Output ripple

For discontinuous conduction, either converter's output ripple can be calculated by equating energy change in the inductor or transformer with energy change in the output capacitor during the off-cycle. Because the inductor/transformer has zero energy at the end of the cycle, no-load ripple can be calculated as:

$$\tfrac{1}{2}LI^2 = \tfrac{1}{2}C_{OUT}V_{final}{}^2 - \tfrac{1}{2}C_{OUT}V_{initial}{}^2$$

$$\tfrac{1}{2}LI^2 = \tfrac{1}{2}C_{OUT}(V_{final} - V_{initial}) \times (V_{final} + V_{initial})$$

$$\tfrac{1}{2}LI^2 = C_{OUT}\,\Delta V_{OUT} \times V_{OUT}$$

$$\Delta V_{OUT} = \frac{\tfrac{1}{2}LI^2}{C_{OUT}\,V_{OUT}}$$

For the boost converter L = L_{BST} and I = I_{PK}. For the circuit of Figure 1c, L = L_{BST} x N and I = I_{PK}/N, so:

$$\Delta V_{OUTA} = \frac{\tfrac{1}{2}L_{BST}(I_{PK})^2}{CV_{OUT}}$$

$$\Delta V_{OUTC} = \frac{\tfrac{1}{2}N \times L_{BST}(\frac{I_{PK}}{N})^2}{CV_{OUT}} = \frac{\Delta V_{OUTA}}{N}$$

where ΔV_{OUTA} is the output ripple of the boost configuration, and ΔV_{OUTC} is the output ripple for the Figure 1c circuit. Ripple in Figure 1c is 1/Nth as large for the boost configuration and the switching frequency is N times higher.

Figure 5 offers a comparison of ripple for the circuits of Figures 1a and 1c, when both circuits are designed for the same off-time. Because the duty cycle is normalized in the transformer circuit (made closer to 50%), the controller can operate at a frequency N times higher for the same off-time.

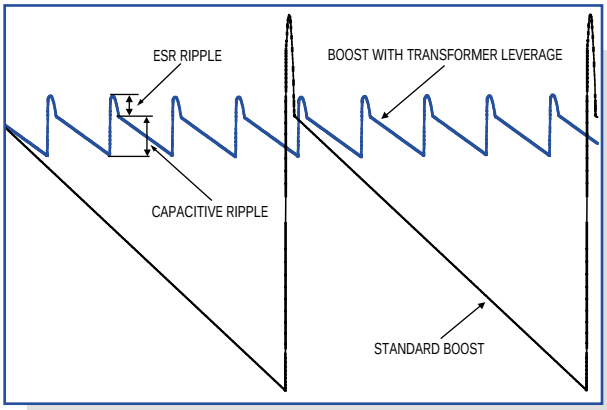


Figure 5. This illustration contrasts the ripple produced by the circuit of Figure 1a vs. the circuit of Figure 1c assuming both are optimized for a minimum acceptable off-time.

Efficiency considerations

There are three main efficiency losses to consider in the transformer topology. Transformer/inductor DC resistance combined with switch resistance produces losses proportional to the square of the peak current. Transformer-leakage inductance produces loss because transformer energy is not completely coupled to the output. When the diode is quickly and heavily reverse-biased (when the MOSFET turns on), any delay in the diode (the reverse-recovery time, t_{RR}) can also cause significant loss.

The percent efficiency loss due to DC resistance in the switch and in the primary side of the transformer is independent of load, and can be approximated as:

$$\frac{E_{R\_LOSS}}{E_{R\_LOSS} + E_{delivered}} \times 100\%$$

where E_{R_LOSS} is the energy loss due to resistance per pulse, and $E_{delivered}$ is the energy delivered per pulse. By taking the integral of the primary-side resistive power dissipation, the resistive efficiency loss for large duty cycles can be approximated as:

$$\frac{\tfrac{1}{3}I_{PK}R}{\tfrac{1}{3}I_{PK}R + \tfrac{1}{2}V_{IN}} \times 100\%$$

where D is the duty cycle expressed as a percentage, and R is the sum of the switch resistance and the primary-side resistance. For operation in discontinuous mode, the same equation applies for the circuit of Figure 1a or 1c. The efficiency loss due to leakage inductance can be approximated as:

$$\frac{L_{leakage}}{L_{leakage} + L_{primary}} \times 100\%$$

where $L_{leakage}$ is the total leakage inductance seen at the primary side. Transformers with higher turns ratios provide larger leakage inductance, higher frequency, and deliver lower energy per pulse, so the source of inefficiency becomes more significant.

Transformer selection

Since the selection of off-the-shelf transformers is much narrower than that of equivalent inductors, transformers generally cost more than inductors of equivalent energy and energy density. The customer base for transformers is smaller, yet the set of possible transformer configurations is much larger than that of corresponding inductor configurations. As a result, magnetic designs based on custom transformers are often necessary.

When specifying an autotransformer, consider an equivalent inductor. The following inductor, for example, is available from Toko: D32FU 680µH, 74mA, 20Ω, 3.5mm x 3.5mm x 2.2mm. It is reasonable to ask for an autotransformer whose end-to-end characteristics are similar. For such a transformer with a 1:9 turns ratio, the primary-side rating would be 6.8µH, 740mA, and 2Ω. That inductance rating is based on a value of N^2 (where N is the total number of turns divided by the number of primary-side turns). For a 1:9 turns ratio there must be some multiple of 10 turns total. N = 10 must be used for the previous calculation. The saturation current is inversely proportional to N and resistance is proportional to N.

Occasionally, thermal limitations do not allow the maximum current rating to scale by N. Also, a limited product selection may bar you from that ideal starting point. This analysis provides a starting point and a decent edge when discussing possibilities with a custom transformer vendor. When wound as an autotransformer, an equivalent magnetic component should require less space (a smaller wiring cavity) because the lower currents allow thinner wire on the secondary side. (Extra manufacturing costs usually prohibit this approach, however.)

Application

The circuit of **Figure 6** produces an APD bias of 75V. Because the transformer reduces voltage stress on the switch, you can use a small 6-pin SOT23 device such as the MAX1605. The 28V, 500mA MOSFET in that IC is more than adequate since it only sees peak voltages of $V_{IN} + (V_{OUT} - V_{IN}) / N = 17V$. With a higher turns ratio, the circuit can handle higher voltages.

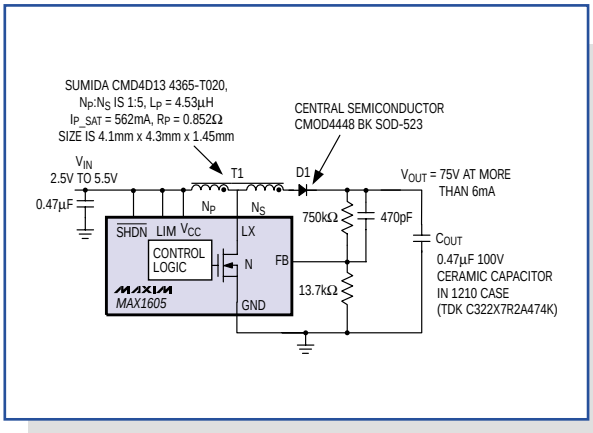


Figure 6. This circuit, whose layout is shown in Figure 2, is used to produce 75V from 2.5V.

Figure 7 shows the MAX1605 maximum output current (the measured typical, for which the controller falls out of regulation by 5%) as a function of output voltage and input voltage.

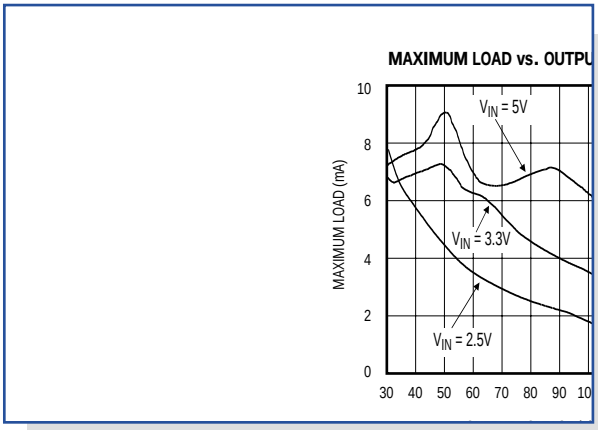


Figure 7. This Maximum Load vs. Output Voltage graph illustrates the maximum load deliverable by the circuit of Figure 6.

Output ripple for the circuit of Figure 1c can be calculated as:

$$V_{RIPPLE} = \frac{\frac{1}{2} L_P \times I_{PK}^2}{C_{OUT} \times V_{OUT}}$$

where L_P is the primary-side inductance, I_{PK} is the peak primary-side current (500mA), C_{OUT} is the output capacitance (0.47µF), and V_{OUT} is the output voltage. For a 75V output, the ripple is $16mV_{P-P}$. The low inductance that produces such a low ripple is typically not efficient in a straight boost configuration like Figure 1a.

Even $16mV_{P-P}$ ripple is not small enough for many applications. To bias an APD, high ripple is unacceptable because it couples directly into the signal. Such applications can use an RC or LC filter following the power supply, but the resistor in an RC filter produces a load-regulation error. (Typical load currents are small, but the ripple filter may require large resistors.)

At 100V, high-capacitance values require board space, so the filter is composed largely of resistance. For the same cutoff frequency (using the same resistor and capacitor), you can reduce the load-regulation error by a factor of β using the circuit of **Figure 8**. Although a fixed V_{BE} drop is introduced instead, that approach dramatically reduces the dependence of V_{OUT} on load. To achieve greater ripple reduction for the same level of load regulation, a β-times larger filter resistor can be used.

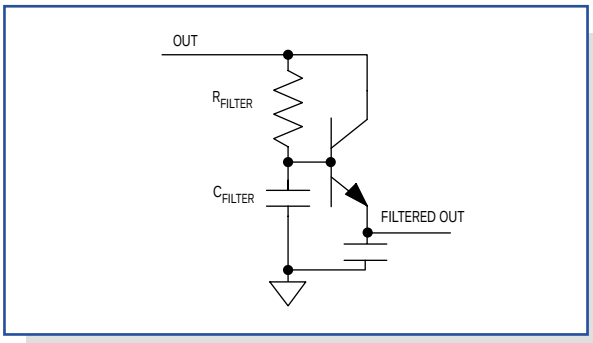


Figure 8. A filter further reduces ripple.

Experimental comparison: inductor and transformer approaches

For a fair comparison of inductors versus transformers in a high-voltage converter, a switching converter with the following features was selected:

- External MOSFETs
- Adjustable switching frequency
- Adjustable current limit
- Evaluation kit available

The MAX668 current-mode controller fulfills these criteria while eliminating the need for a feedforward capacitor. The circuit of **Figure 9** allows you to compare performance by swapping the transformer for an inductor and by swapping MOSFETs.

The MAX668 includes a MOSFET driver that can efficiently drive the 48nC gate charge of an IRF7401 MOSFET. With the following components, it forms a 150V inductor-based boost converter. The following components were used in conjunction with the MAX668 Evaluation Kit:

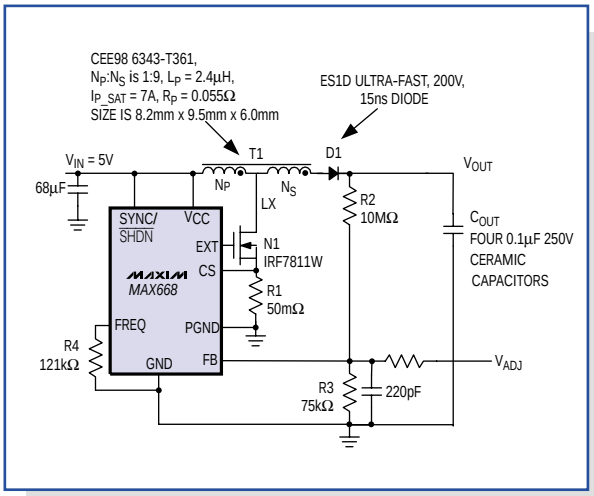


Figure 9. This circuit can be used to deliver higher power and higher output voltage.

- Inductor: Coilcraft DO1813P-472HC 4.7µH, 2.6A 0.054Ω inductor
- Ultra-fast diode: ES1D 200V 15ns reverse-recovery time
- MOSFET: IRF640NS 200V 0.15Ω Q_G = 67nC, C_{OSS} = 185pF, and provides over 2A with 5.5V gate drive
- Sense resistor: 50mΩ sense resistor

Another resistor connected between the FB terminal and a voltage source allows that source to adjust the output voltage by sinking or sourcing current to the FB terminal. You can then adjust the output voltage to 150V and the input voltage to 6V.

For the inductor-based solution, the maximum load current is 18mA at 150V (2.7W). Peak efficiency (65%) occurs at maximum load and the quiescent (no-load) current is 91mA with a 6V supply. The quiescent-current loss in the inductor circuit is due to the diode's reverse-recovery time and the MOSFET's drain capacitance. Those effects are illustrated in **Figure 10**.

The transformer-based approach **(Figure 11)** was implemented by exchanging the inductor for the following transformer, using the topology of Figure 1c:

Sumida CMD-8LN 6313-T036,
L_P = 5.6µH, I_P = 2.3A, N_P:N_S = 1:9,
R_P = 0.5Ω

Using a transformer with a 1:9 turns ratio requires only a 22V MOSFET, but an actual application would use a 30V MOSFET (instead of a 200V MOSFET) for the transformer circuit. Yet, the efficiency is 77% while delivering 25.5mA at 150V (3.8W). Peak efficiency is 88% at 15mA, and the no-load supply current is only 1.8mA total.

Using the 200V MOSFET with a transformer allows the possibility of much higher voltage. A 200V MOSFET and 1:9 transformer can approach output voltages as high as 2kV in theory, but in practice the transformer windings cannot sustain such high voltage. A greater problem, however, is obtaining >1kV diodes with fast reverse-recovery times. For slow reverse-recovery times, the switching speed must be reduced.

Substituting a 400V CMR1U-04 diode from Central Semiconductor (50ns t_{RR}) for the ES1D diode and changing the output capacitors allows the circuit to produce outputs as high as 400V. The ES1D diode cannot reliably produce outputs greater than 346V, because its anode goes to -9 x V_{IN} when the MOSFET

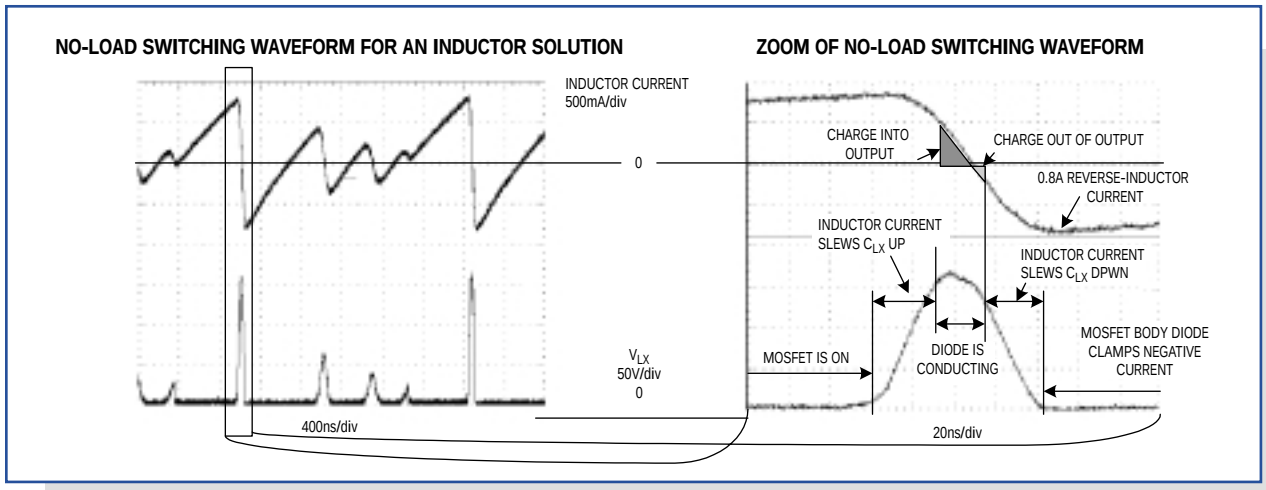


Figure 10. This scope photo (left) demonstrates the effect of the ES1D diode's 15ns reverse-recovery time. The zoom of the waveform (right) reveals that the inductor current actually ramps negative since the diode fails to turn off in time.

turns on. Configured for V_{OUT} = 330V, the circuit was able to produce 9.6mA (3.1W) at 60% efficiency and the peak efficiency was 66% at 4mA.

As mentioned earlier, a 30V MOSFET is more logical for the 150V output. The IRF640NS was replaced with a logic-level IRF7811W (30V, 0.012Ω, Q_G = 18nC, C_{DSS} = 500pF). Resistance drops dramatically (from 0.15Ω to 0.012Ω), but the efficiency improvement is minor. When delivering a maximum load of 25.7mA at 150V, the efficiency is 82.3% (vs. 77%). Peak efficiency at 15.5mA is 88%. Efficiency results are summarized in **Figure 12.**

The insignificant improvement in efficiency implies two things. Primary losses are in the transformer (resistive loss and leakage energy), and capacitive losses are in the MOSFET. The dominant loss is associated with the transformer's primary-side resistance, which is about 0.5Ω. You can scale this system to provide higher power. For example, another custom transformer specified for I_{PSAT} = 5A and L_P = 1.7µH should deliver more than twice as much power.

Thus, besides use of the smaller, cheaper, and more efficient IRF7811W MOSFET, a transformer boost converter can operate with lower input voltages. Transformer leverage can improve power density and efficiency, reduce ripple, and allow the use of smaller, cheaper, and sometimes internal MOSFETS. The cost of applying transformer leverage is mostly due to market limitations. When size and power density are a high priority, consider using transformers.

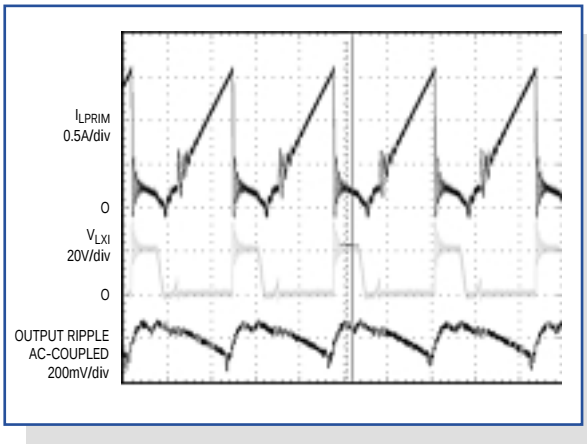


Figure 11. The switching waveform shows the transformer-based approach for the MAX668 circuit, a 150V step-up DC-DC converter shown in Figure 9.

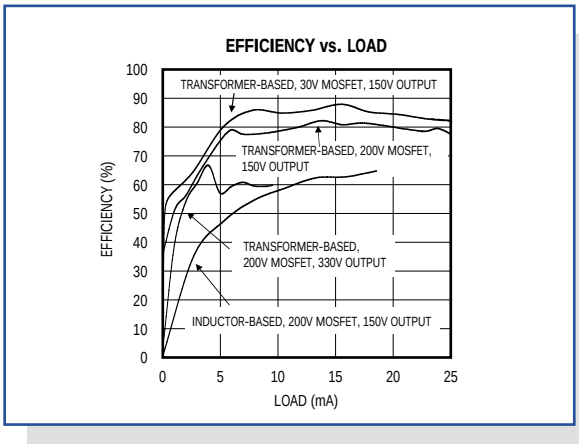


Figure 12. This Efficiency vs. Load graph compares and contrasts transformer-based, step-up DC-DC converters vs. inductor-based, step-up DC-DC converters. The maximum load, quiescent current, and efficiency are greatly improved using a transformer.

Compact, inductorless boost circuit regulates white-LED bias current

The increasing use of color LCDs in hand-held equipment is creating a need for smaller and cheaper sources of white backlight. Cold-cathode fluorescent lamps (CCFLs) and electro-luminescent (EL) panels have been used in the past, but those circuits are excessively large, expensive, and complex for today's hand-held, consumer-electronics devices. Fortunately, recent advances in LED technology have produced an LED that emits white light. White LEDs have several advantages over conventional backlights, including small size, low cost, low complexity, and high reliability.

The typical forward-bias voltage for white LEDs is about 3.5V ±10%. To obtain white light, you simply forward-bias the device, but a boost circuit is required if the white LED's forward voltage can be greater than the battery voltage. The conventional approach to this problem—a boost regulator that biases the LEDs through a ballast resistor—has two drawbacks. First, the wide variation of forward voltage in white LEDs causes a large variation in bias current and the resulting light output. Second, the conventional boost converter has a DC path between input and output (even in shutdown) that allows an inactive LED to drain the battery.

Figure 1's compact circuit overcomes these problems. The regulated buck/boost charge pump in a small µMAX package (U1) has a 100mA output-current capability. Configured as shown, the circuit directly regulates bias current flowing through the white LED. By biasing multiple white LEDs in parallel, it provides good light distribution. The U1's design eliminates the troublesome input-output path in shutdown, and its $\overline{SHDN}$ input lets the user turn the backlight on and off. The circuit also includes a power-OK (POK) output for signaling a microprocessor when the backlight is available.

Though not necessary in this case, the input RC "π" filter limits voltage ripple reflected back to the input to just $40mV_{P-P}$ (for V_{IN} = 3.6V). Because output-voltage ripple is not visible to the eye, it is of secondary concern in this application and allows the use of a small (0.22µF) output capacitor. Even so, the output ripple is only $400mV_{P-P}$.

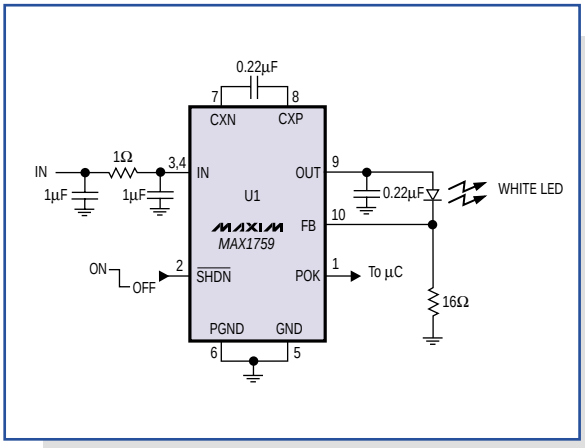


Figure 1. Unorthodox connections enable this regulated charge-pump IC to directly regulate the white LED's bias current.

(A similar idea appeared in the 3/5/01 issue of *Electronic Design*.)

Analog switch lowers relay power consumption

Relays are often used as electrically controlled switches. Unlike transistors, their switch contacts are electrically isolated from the control input. On the other hand, the power dissipation in a relay coil may be unattractive for battery-operated applications. Adding an analog switch lowers the dissipation, allowing the relay to operate at a lower voltage **(Figure 1)**.

Power consumed by the relay coil equals V^2/R_{COIL}. The circuit lowers this dissipation (after actuation) by applying less than the normal operating voltage of 5V. Note that the voltage required to turn a relay on (pickup voltage) is greater than that required to keep it on (dropout voltage). The relay shown has a 3.5V pickup voltage and a 1.5V dropout voltage, yet the circuit allows it to operate from an intermediate supply voltage of 2.5V. **Table 1** compares the relay's power dissipation with fixed-operating voltages across it, and with the Figure 1 circuit in place.

By closing SW1, current flows in the relay coil, and C1 and C2 begin to charge. The relay remains inactive because the supply voltage is less than its pickup voltage. The RC time constants are such that C1 charges almost completely before the voltage across C2 reaches the logic threshold of the analog switch.

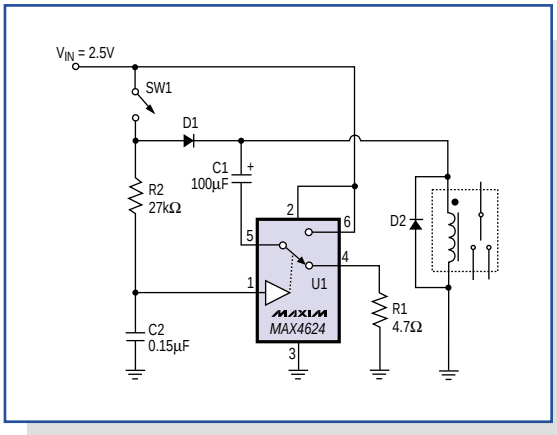


Figure 1. An analog switch lowers relay power dissipation.

Table 1. Power dissipated by relay

Voltage (V)	Current (mA)	Total Power Dissipation (mW)
5 (Normal OperatingVoltage)	90	450
3.5 (Pickup Voltage)	63	221
2.5 (Circuit of Figure 1)	45	250

When C2 reaches that threshold, the analog switch connects C1 in series with the 2.5V supply and relay coil. This action turns on the relay by boosting the voltage across its coil to 5V (twice the supply voltage). As C1 discharges through the coil, the coil voltage drops back to 2.5V minus the drop across D1, but the relay remains on because that voltage is above the relay's dropout voltage (1.5V).

Component values for this circuit depend on the relay characteristics and the supply voltage. The value of R1, which protects the analog switch from the initial current surge through C1, should be sufficiently small to allow C1 to charge rapidly, but large enough to prevent the surge current from exceeding the specified peak current for the analog switch. The switch's peak current (U1) is 400mA, and the peak surge current is $I_{PEAK} = (V_{IN} - V_{D1})/(R1 + R_{ON})$, where R_{ON} is the on-resistance of the analog switch (typically 1.2Ω). C1's value depends on the relay characteristics and on the difference between V_{IN} and the relay's pickup voltage. Relays that need more turn-on energy require larger C1 values.

The values for R2 and C2 are selected to allow C1 to charge almost completely before C2's voltage reaches the logic threshold of the analog switch. In this case, the time constant C2R2 is about seven times C1(R1 + R_{ON}). Larger C2R2 values increase the delay between switch closure and relay activation.

(A similar idea appeared in the 12/20/01 issue of *EDN*.)